What is claim d is:

1. A current sense apparatus using a combination of a simulation and a real sense for generating a current sense signal for a switching mode DC-to-DC power converter having a high-side transistor connected between an input voltage and an output node, and a low-side transistor connected between the output node and a reference potential, to provide an output voltage and an output current from the output node through an inductor, the apparatus comprising:

a ramp signal generator for generating a ramp signal with a slope proportional to a difference between the input and output voltages during each first half cycles of a clock;

a DC signal generator for generating a DC signal proportional to a DC component of a current through the low-side transistor by measuring the current through the low-side transistor; and

a summing circuit for combining the ramp and DC signals to generate the current sense signal.

2. The apparatus of claim 1, wherein the ramp signal generator comprises:

a current source for providing a charging current; and

a capacitive element charged by the charging current for generating the ramp signal.

3. The apparatus of claim 2, wherein the charging current is proportional to the difference.

4. The apparatus of claim 2, wherein the current source comprises:

a second summing circuit having a positive input connected with the input voltage and a negative input connected with the output voltage for generating the difference; and

a transconductive amplifier for transforming the difference to the charging current.

5. The apparatus of claim 2, wherein the ramp signal generator further comprises a switch between the current source and capacitive element controlled by the clock for connecting the charging current to the capacitive element.

6. The apparatus of claim 1, wherein the DC signal generator comprises:

a resistive element connected between the low-side transistor and reference potential for generating a voltage drop;

a measurement circuit for generating a measurement signal from the voltage drop; and

a sample and hold circuit for sampling and holding the measurement signal at each ends of the clock to generate the DC current signal.

7. The apparatus of claim 1, wherein the DC signal generator comprises:

a measurement circuit for generating a measurement signal from a voltage drop across the low-side transistor; and

a sample and hold circuit for sampling and holding the measurement signal at each ends of the clock to generate the current signal.

8. A current sense method using a combination of a simulation and a real sense for generating a current sense signal for a switching mode DC-to-DC power converter having a high-side transistor connected between an input voltage and an output node, and a low-side transistor connected between the output node and a reference potential, to provide an output voltage and an output current from the output node through an inductor, the method comprising the steps of:

measuring a current through the low-side transistor for generating a DC signal proportional to a DC

component of the current through the low-side transistor;

generating a ramp signal with a slope proportional to a difference between the input and output voltages during each first half cycles of a clock; and

combining the ramp and DC signals for generating the current sense signal.

9. The method of claim 8, wherein the step of generating a ramp signal comprises charging a capacitive element by a charging current.

10. The method of claim 9, further comprising generating the charging current proportional to the difference between the input and output voltages.

11. The method of claim 10, wherein the generation of the charging current comprises:

subtracting the output voltage from the input voltage for generating the difference; and

transforming the difference to the charging current.

12. The method of claim 9, further comprising using the clock to control the charging current to connect to the

capacitive element.

13. The method of claim 8, wherein the generation of the DC current signal comprises:

arranging a resistive element between the low-side transistor and reference potential for generating a voltage drop;

generating a measurement signal from the voltage drop; and

sampling and holding the measurement signal at each ends of the clock for generating the DC signal.

14. The method of claim 8, wherein the generation of the DC signal comprises:

measuring a voltage drop across the low-side transistor;

generating a measurement signal from the voltage drop; and

sampling and holding the measurement signal at each ends of the clock for generating the DC signal.